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Harmonics Study and Comparison of Z-source Inverter with Traditional Inverters

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Abstract: This paper presents an Impedance Source Inverter for A.C electrical drives. The impedance source inverter employs a unique impedance network cable with inverter main circuit and rectifier. By controlling the shoot-through duty cycle, the z-source inverter system using MOSFETS provide ride-through capability during voltage sags, reduces line harmonics, improves power factor and high reliability, and extends output voltage range. Analysis, simulation, and experimental results will be presented to demonstrate these new features. It reduces harmonics, electromagnetic interference noise and it has low common mode noise.

Key words: Line harmonics, motor drives, voltage sags, Z-source inverter

INTRODUCTION

The traditional inverters are VOLTAGE SOURCE INVERTER (VSI) and Current Source Inverter (CSI). Which consists of a diode rectifier front end, dc link and inverter bridge. In order to improve power factor, either an ac inductor or dc inductor is normally used. The dc link voltage is roughly equal to 1.35 times the line voltage, and the V-source inversion is a buck converter that can only produce an ac voltage limited by the dc link voltage. Because of this nature, the V-source inverter based PWM VSI and CSI are characterized by relatively low efficiency because of switching losses and considerable EMI generation. Since switches are used in the main circuit, each is traditionally composed of power transistors and anti parallel diode. It provides bi-directional current flow and unidirectional voltage blocking capability. Thus inverter presents negligible switching losses and EMI generation at the line frequency. The tackle which exists in the voltage inverter are an output LC filter needed to provide sinusoidal voltage compared with current source inverter. The LC filter causes additional power loss and controlled complexity. To avoid short circuiting of damaging dead line is allowing which provides a delay time between gating signals but it causes waveform distortion.

The ASD system suffers the following common limitations and problems. Obtainable output voltage is limited quite below the input line voltage. The diode rectifier fed by the 415-V ac line produces about 560-V dc on the dc-link , which is roughly 1.35 times the line-to-line input voltage under the assumption of heavy load and continuous “double –hump” input current for large (>50kW) drives that typically have an approximately 3% of inductance on the ac or dc side.

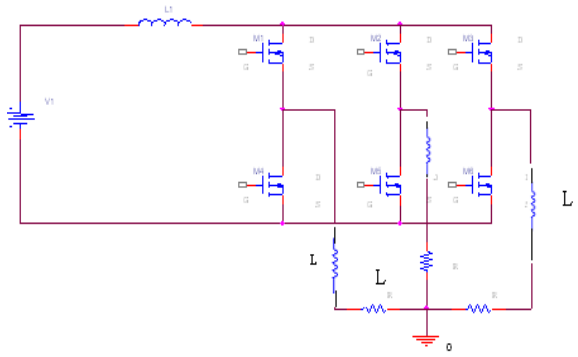

Fig. 1: Power conversion

For light load operation or small drives with no significant inductance, the line current becomes discontinuous “double-pulse,” and the dc voltage is closer to 1.41 times the line –to-line input voltage 400-V motor, the low obtainable output voltage significantly limits output power that is proportional to the square of the voltage. This is a very undesirable situation for many applications because the motor and drive system has to be oversized for a required power. Voltage sags can interrupt an ASD system and shut down critical loads and processes. Over 90% of power quality related problems are from momentary (typically 0.1-2s) voltage sags of 10-50% below nominal. The dc capacitor in droves is a relatively small energy storage element, which cannot hold dc voltage above the operable level under such voltage sags. Lack or ride through capacity is a serious problem for sensitive loads driven by drives[1-11]. Duran *et al.*[11] details the vulnerability of a drive and the dc voltage under three-phase and two phase voltage sag .Solutions have been sought to boost ride–through[2-11]. The drives industry provides options using fly back converter or boost converter with energy storage or a diode rectifier (Fig. 3)

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to achieve ride-through; however, these options come with penalties of cost, size/weight, and complexity.

Inrush and harmonic current from the diode rectifier can pollute the line. Low power factor is another issue of the traditional drives.

Performance and reliability are compromised by the V-source inverter structure, because miss-gating from EMI can cause shoot-through that leads to destruction of the inverter, the dead time that is needed to avoid shoot-through creates distortion and unstable operation at low speeds, and common-mode voltage causes shaft current and premature failures of the motor. A recently developed new inverter, the z-source inverter[1], has a niche for drive systems to overcome the aforementioned problems [11]. A Z- source inverter based drives can:

* produce any desired output a voltage, even greater than the line voltage, regardless of the input voltage, thus reducing motor ratings;
* provide ride-through during voltage sags without any additional circuits;
* improve power factor reduces harmonic current and common-mode voltage.

Impedance source inverter: This Impedance source inverter is used to overcome the problems in the traditional source inverters. This impedance source inverter employs a unique impedance network coupled with the inverter main circuit to the power source. This inverter has unique features compared with the traditional sources.

It consists of voltage source of the rectifier supply, Impedance network, three phase inverter and with A.C. motor load**.** An AC voltage is rectified to DC voltage from the rectifier. In the rectifier unit consist of six diodes, which are connected in a bridge way. This rectified output DC voltage fed to the impedance network.

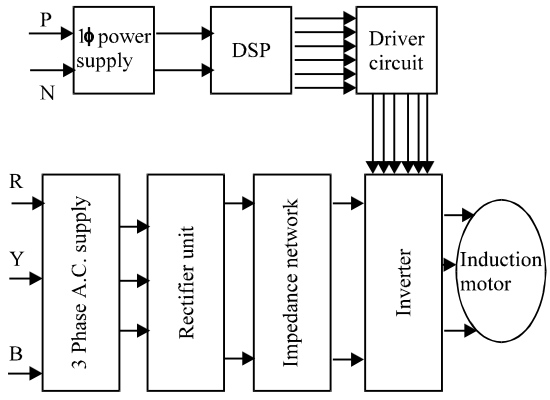

Fig. 2: Block diagram of the impedance source inverter

Which consist of two equal inductors (L1, L2) nd two equal capacitors (C1, 2). The network inductors are connected in series arms and capacitors are connected in diagonal arms. The impedance network used buck or boost the input voltage depends upon the boosting factor. This network also acts as a second order filter .This network should require less inductance and smaller in size. Similarly capacitors required less capacitance and smaller in size. This impedance network, the constant impedance output voltage fed to the three phase inverter main circuit. The inverter main circuit consists of six switches .Gating signals are generated from the DPWM. Which to generated by digital signal processor. The discontinuous pulse width modulation (DPWM) will minimize the harmonic content This signals fed to the MosFET Gate terminals .Depends upon the Gating signal inverter operates, this output fed to the AC load or motor.

Impedance Network: The lattice networks are used in filter sections and are also used as attenuators. Lattice networks are sometimes used in preference to ladder structure in some special applications. This lattice network, L1 and L2 are series arms inductances, C1 and C2 are diagonal capacitances. This is a two-port network that consists of split inductors L1 and L2 and capacitors C1 and C2 connected in X-shape. This network is coupled with the main circuits and the source, to describe the operating principle of inverter in Fig. 3. The three-phase impedance source inverter bridge has nine permissible switching states unlike the traditional voltage source inverter that has eight switching states. The impedance source inverter bridge has one extra zero state. When the load terminals are shorted through both upper and lower devices of any one phase lag or all three phase legs. This shoot through the zero state is forbidden in the VSI, because it would cause a shoot- through. This network makes the shoot through zero state possible. This state provides the unique buck-boost feature to the inverter.

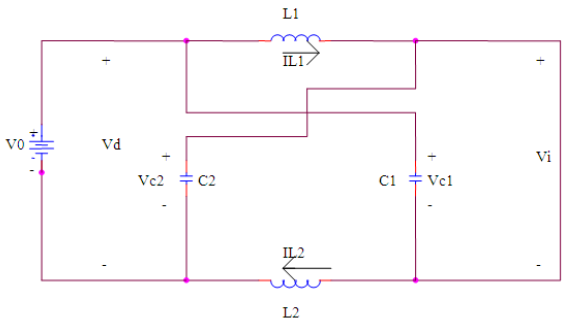

Fig. 3: Equivalent circuit of the impedance-source inverter

Comparison of VSI, CSI and ZSI

Current Source Inverters	Voltage Source Inverter	Impedance Source Inverters
1. As inductor is used in the d.c link, the source impedance is high. It acts as a constant current source.	As capacitor is used in the d.c link, it acts as a low impedance voltage source.	As capacitor and inductor is used in the d.c link, it acts as a constant high impedance voltage source.
2. A current source inverter is capable of withstanding short circuit across any two of its output terminals. Hence the momentary short circuit on loads and misfiring of switches are acceptable.	A VSI is a more dangerous situation as the parallel capacitor feeds more powering to the fault.	In ZSI misfiring of the switches sometimes are also acceptable.
3. This is used in only buck or boost operation of the inverter.	This is also used in only a buck or boost operation of the inverter.	This is used in both buck and boost operation of the inverter.
4. The main circuits cannot be interchangeable.	The main circuit cannot be interchangeable here also.	Here the main circuits are interchangeable
5. It is affected by the EMI noise.	It is affected by the EMI noise	It is less affected by the EMI noise.
6. It has a considerable amount of harmonic distortion	It has a considerable amount of harmonic distortion	Harmonics Distortion in low
7. Power loss should be higher because of the filter	The power loss is high	Power loss should be low
8. Lower efficiency because of high power loss	Efficiency should be lower because of power loss high	Higher efficiency because of less power loss

Mode I: The inverter bridge is operating in one of the six traditional active vectors, thus acting as a current source (i_i) viewed from the z-source circuit. The diodes (D_{pa} and D_{nb}) conduct and carry currents. In the traditional ASD system, the diode bridge may not conduct depending on the dc capacitor voltage level. However, the Z-source circuit always forces diode (D_{pa} and D_{nb}) to conduct and carry the current difference between the inductor current (I_{ld}.) and inverter dc current (i_i), d_{IL}d-i_i). Note that both industries have an identical current value because of the circuit symmetry. This unique feature widens the line current conducting intervals, thus reducing harmonic current.

Mode II: The inverter bridge is operating in one of the two traditional zero vectors and sorting through either the upper or lower three devices, thus acting as an open circuit viewed from the Z-source circuit. The diodes (D_{pa} and D_{nb}) conduct and carry currents. Again, under this mode, the two diodes (D_{pa} and D_{nb}) have to conduct and carry the inductor current, which contributes to the line current's harmonic reduction.

Mode III: The inverter bridge is operating in one of the seven shoot through the states. During this mode, both diodes are off, separating the dc link from the ac line. The line current flows into the capacitor (CA). This is the shoot-through mode to be used every switching cycle during the traditional zero vector period generated by the PWM control. Depending on how much a voltage boost is needed, the shoot-through interval (T_0) or its duty cycle (T_0/T) is determined[7]. It can be seen that can be seen that the shoot-through interval is only a fraction of the switching cycle; therefore it needs a relatively small capacitor (C_a) to suppress voltage.

In summary, there are six diode conduction. Rectification intervals per line cycle that are determined by the line side voltage; each interval has three operating modes that are determined by the inverter bridge's switching states. The shoot-through switching states provide both challenges and opportunities in terms of PWM control. A simple PWM control for the Z-source inverter bridge was proposed[7] and more sophisticated control methods can be found[8,9]. The following paragraph will describe the shoot-through operation in more detail and provide a summary of the theoretical relationships.

The operating principle and control of the Z-source inverter itself have been detailed[7]. The traditional three-phase V-source inverter has six active states in which the DC voltage is impressed across the load and two zeroes states, in which the load terminals are shorted through either the lower or upper three devices, respectively. However, the three-phase Z-source inverter bridge has additional zero states when the load terminals are shorted through both the upper and lower devices of any one phase leg (i.e., both devices are gated on), any two phase legs, or all the three phase legs. These shoots-through zero states are forbidden in the traditional V-source inverter, because it would cause a shoot-through states via any one phase leg, three shoot-through states from combinations of any two phase legs, and one shoot-through state by all the three phase legs. The shoot-through zero states boost dc capacitor voltage while producing no voltage to the load. It should be emphasized that both the shoot-through zero states and the two traditional zero states short the load terminals and produce zero voltage across the load, thus preserving the same PWM properties and voltage waveforms to the load. The only difference is the shoot –through zero states boost the DC capacitor voltage, whereas the traditional PWM inverter without a shoot-through when a desired output voltage is less than 190-v AC, which is the maximum voltage

obtainable from the 400-V line using the linear region PWM. The diode rectifier produces about 560 V across the dc capacitors (C_1 and C_2). When a higher output voltage is required or when the line voltage is experiencing sags, the shoot –through zero states are employed to boost the dc capacitor voltage. The longer time the shoot-through zero states are used, the higher voltage one gets. By controlling the shoot-through zero state intervals, a desired dc voltage can be maintained. All the relationships described in detail[7] about the dc capacitor voltage, shoot-through time interval (or duty cycle), and output voltage hold true for the proposed ASD system.

Inductor and capacitor requirements: The Impedance source network is a combination of two inductors and two capacitors. This combined circuit; the impedance source network is the energy storage or filtering element for the Impedance source inverter. This impedance source network provides a second order filter. This is more effective to suppress voltage and current ripples. The inductor and capacitor requirement should be smaller compare than the traditional inverters. The two inductors (L1 and L2) are small and approach zero, the Impedance source network reduces to two capacitors (C1 andC2) in parallel and becomes a traditional voltage source. Therefore, a traditional voltage inverter's capacitor requirement and physical size is the worst-case requirement for the Impedance source inverter. Considering additional filtering and energy storage provided by the inductors, the Impedance source network should require less capacitance and smaller size compare with the traditional voltage source inverter. Similarly, when the two capacitors (C1 and C2) are small and approach zero, the Impedance source network reduces to two inductors (L1 and L2) in series and becomes a traditional current source. Therefore, a current source inverter's inductor requirements and physical size are the worst case requirement for the Impedance source inverter.

The two capacitors are small; the Impedance source network reduces to two inductors in series and becomes a traditional current source. Considering additional filtering and energy storage by the capacitors, the Impedance source network should require less inductance and smaller size compared with the traditional current source inverters.

Analysis and design of the impedance network:

Analysis of impedance network: Assume the inductors (L1&L2) and capacitors (C1 &C2) have the same inductance and capacitance values respectively.

From the above equivalent circuit:

$$V_{c1} = V_{c2} = V_c \quad (1)$$

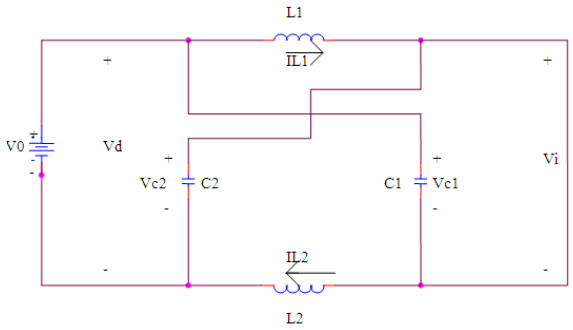

Fig. 4: Equivalent circuit of the impedance network

$$V_{L1}=V_{L2}=V_L \quad (2)$$
$$V_L = V_c,\ V_d = 2V_c$$
$$V_i=0;$$

During the switching cycle T:

$$V_L=V_o-V_c \quad (3)$$
$$V_d = V_o$$

$$V_i= V_c - V_L\ V_c-(Vo-V_c)$$
$$V_i= 2V_c - V_o \quad (4)$$

where, Vo is the dc source voltage and:

$$T=To + T1 \quad (5)$$

The average voltage of the inductors over one switching period (T) should be zero in steady state:

$$V_L = V_L = T_o .V_c + T_1(V_o-V_c)/T = 0$$
$$V_L = (T_o .V_c + V_o.T_1 - V_c.T_1)/T=0$$
$$V_L=(T_o-T_c)V_c/T + (T_1.V_o)/T$$
$$V_c/V_o=T_1/T_1-T_0 \quad (6)$$

Similarly the average dc link voltage across the inverter bridge can be found as follows.

From equation 4:

$$Vi=Vi = (To .0+T_1. (2Vc-Vo))/T \quad (7)$$
$$Vi = (2Vc. T_1/T)-(T_1Vo/T)$$
$$2Vc=Vo$$

From equation 6:

$$T1.Vo/(T1-To) =2Vc. T1/(T1-To)$$
$$Vc=Vo. T1/(T1-To)$$

The peak dc-link voltage across the inverter bridge is:

$$Vi=Vc-Vl=2Vc-Vo$$
$$=T/(T1-To). Vo=B. Vo$$

where, B=T/(T1-To) i.e ≥1
B is a boost factor

The output peak phase voltage from the inverter:

$$Vac=M.vi/2 \quad (9)$$

where, M is the modulation index:

$$InthissourceVac=M.B.Vo/2 \quad (10)$$

In the traditional sources:

Vac = M.Vo/2
For Z-Source
Vac = M.B.Vo/2

The output voltage can be stepped up and down by choosing an appropriate buck-boost factor B_B:

$$B_{B=} B.M \text{ (it varies from 0 to } \alpha) \quad (11)$$

The capacitor voltage can be expressed as:

$$Vc1=Vc2=Vc= (1-To/T). Vo/(1-2To/T)$$

The boost factor B_B is determined by the modulation index m and the boost factor B. The boost factor B can be controlled by duty cycle of the shoot through the zero state over the non-shoot through the states of the PWM inverter. The shoot through zero state does not affect PWM control of the inverter. Because it equivalently produces the same zero voltage to the load terminal. The available shoot through period is limited by the zero state periods that is determined by the modulation index.

Design of impedance (z) network:

Where L1 and L2 - series arm inductors
C1 and C2 - parallel arm capacitors
V1 is input voltage
V2 is the output voltage

The network can be redrawn this way

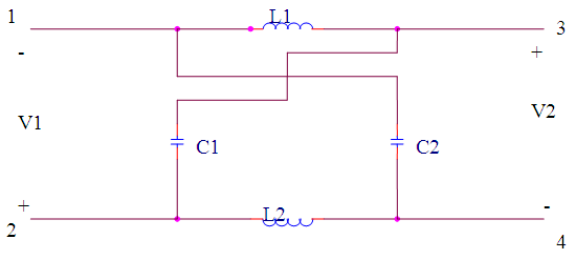

Fig. 5: Impedance network

Now assume $I_2 = 0$, the current I_1enters the bridge at point 1 and divides equally between the two arms of the bridge.

Using Kirchhoff's law:

$$I_1.L/2+V_2 = I_1/2c$$
$$V_2 = I_1/2c - I_1.L/2$$

$$V_2 = I_1/2 [1/c -L]$$

Assume c=5.5 mF
$440 = 5/2 [1/5.5*10^{-3}- L]$
$L = 5.8$ H

$$V_{dc}=BV_0= (2B/B+1) Vc.$$

Simulation and experimental verification of the z-source asd system: To confirm the operating principle of the new ASD system, simulations have been carried out and a 3-KW prototype has been built. In order to show clearly the output voltage obtained from the inverter, an LC filter with 1-kHZ cutoff frequency is placed in between the inverter bridge and the motor. The simulation and experimental system are setup with the following parameters.

Three-phase line voltage: 400V, 3-KW induction motor.

* Load: three –phase KW induction motor.
* Input capacitors (C_a,C_b and C_c): 5.5μF;
* Z-source network: $L_1=L_2=$
* 160μH, $C_1=C_2=$ 1000μF.
* Switching frequency: 10 kHz.

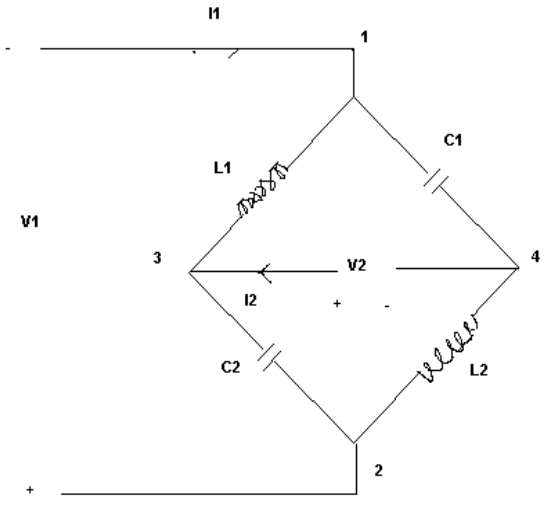

Fig. 6: Impedance network circuit-redrawn

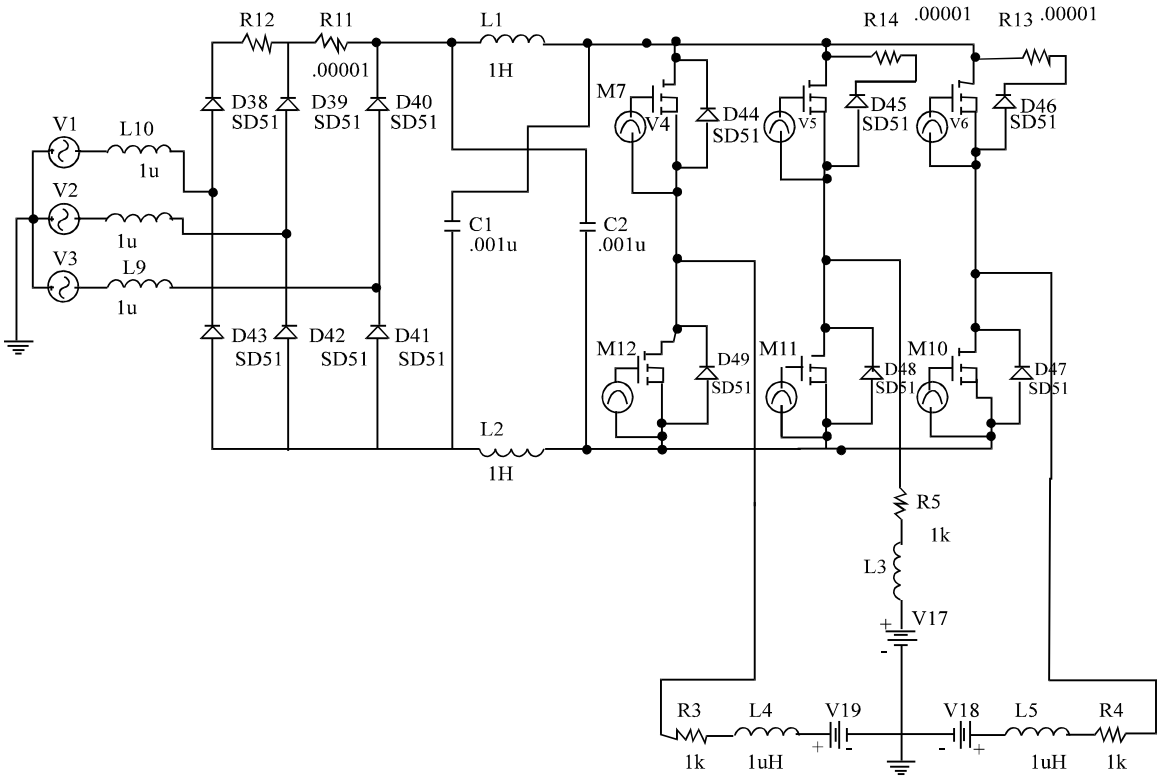

Fig. 7: Impedance source inverter

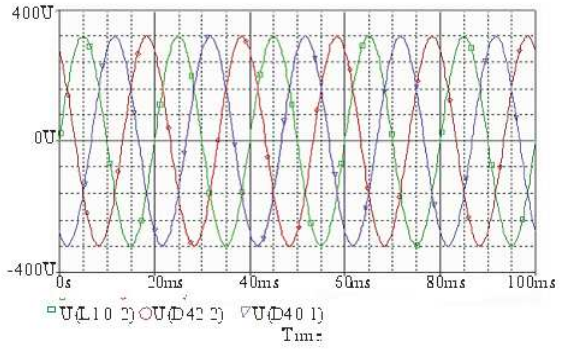

Fig.8.1: Three phase A.C input voltage

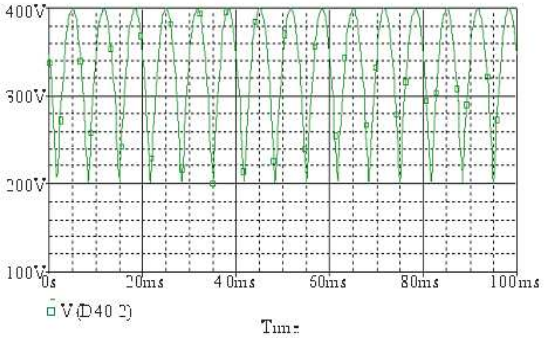

Fig. 8.2:

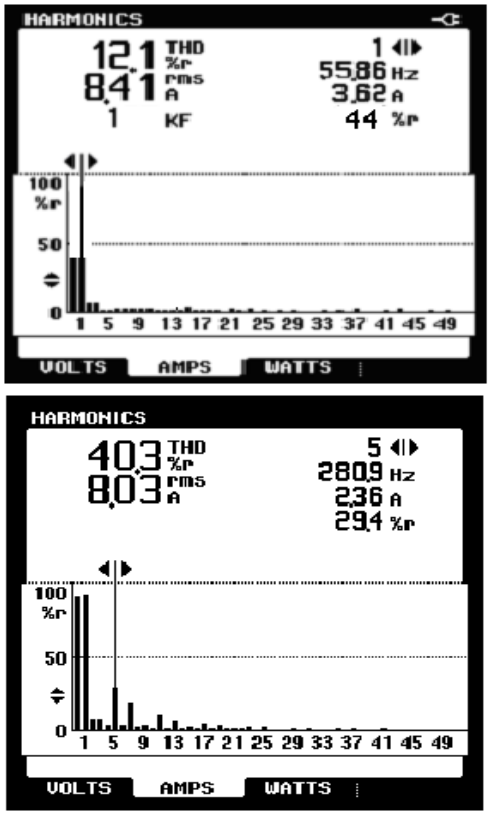

Fig. 9: Current harmonics in traditional inverters

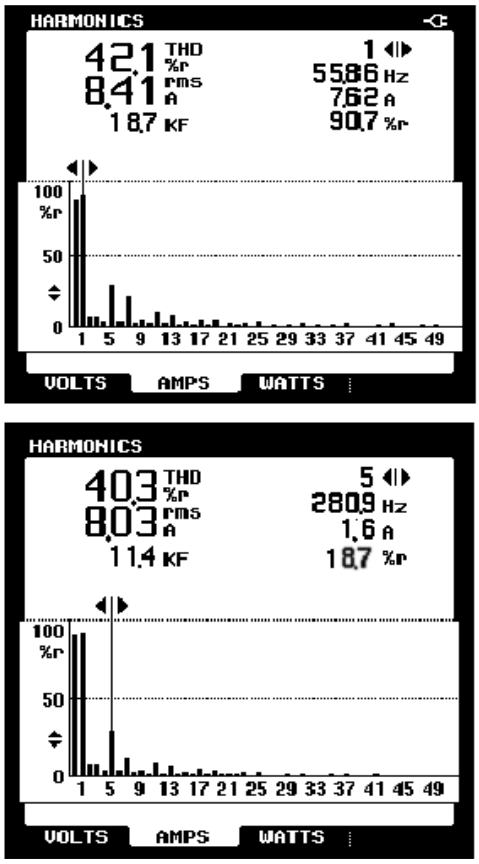

Fig. 10: Current harmonics in z-source inverters

Simulation results of the impedance source inverter: Figure 8.1 shows simulation waveforms under the nominal line voltage of 400-V AC. The inverter modulation index was 1.0, producing the same PWM waveform (VI_{ab}) as the traditional inverter. However, the magnitude of the output voltage was boosted to 415 V rms and was confirmed by the sinusoidal waveform (V_{Lab}) after the 1-kHz LC filter. The traditional PWM inverter cannot produce 400V rms output voltage. The boost factor B was 1.21. Also , it is noted that the line current contains much less harmonics than the traditional ASD system without dc inductors and appreciably less harmonics that the traditional ASD system even with dc inductor because of both the Z-source inductors and input capacitors. Again, the line current harmonics have been reduced greatly.

A prototype has been built to further verify the operation, the critical relationships of voltage boost, and simulation results of the presented Z-source ASD system. It should be noted that the inductors and capacitors were oversized in the prototype for possible regenerative operation during deceleration or inverter trips. The requirement of Z-source network has been discussed[7], which should not differ much from the traditional drives. For large (50 kW or above) drives a dc inductor is commonly used to minimize line harmonic current and voltage distortion.

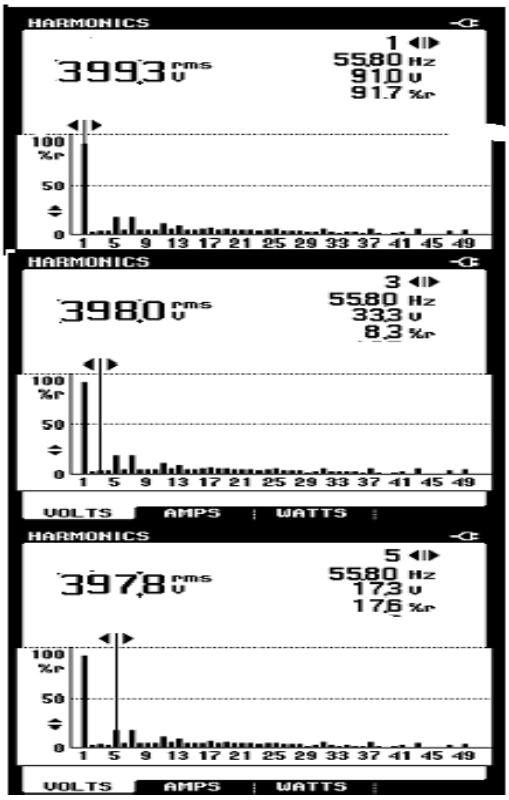

Fig. 11: Voltage harmonics in traditional inverters

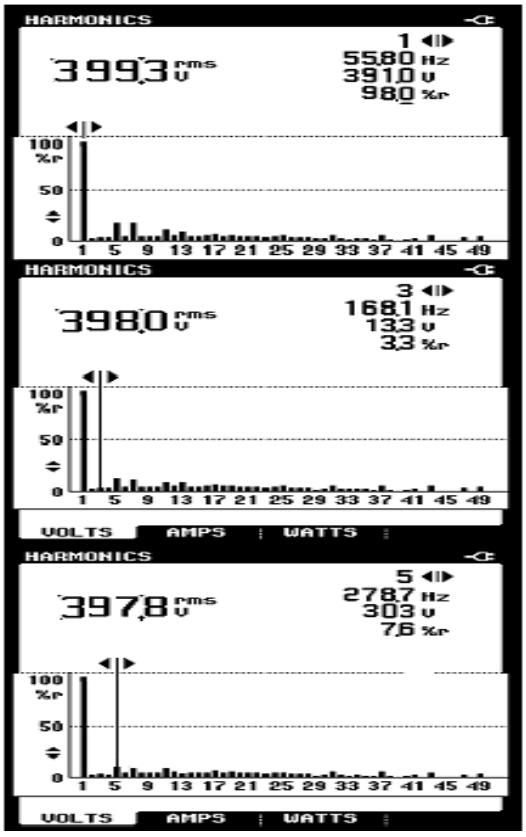

Fig. 12: Voltage harmonics in z-source inverters

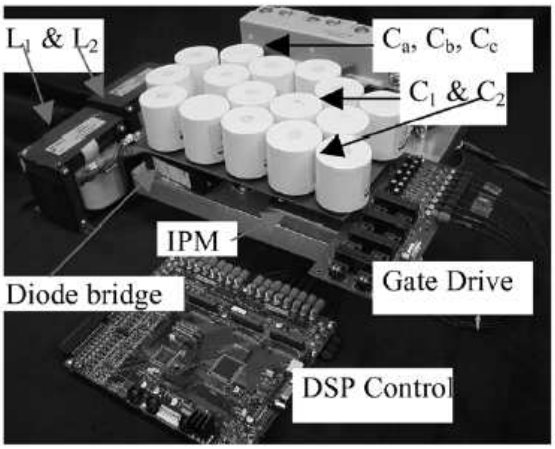

Fig. 13: Prototype of the Z-source ASD system

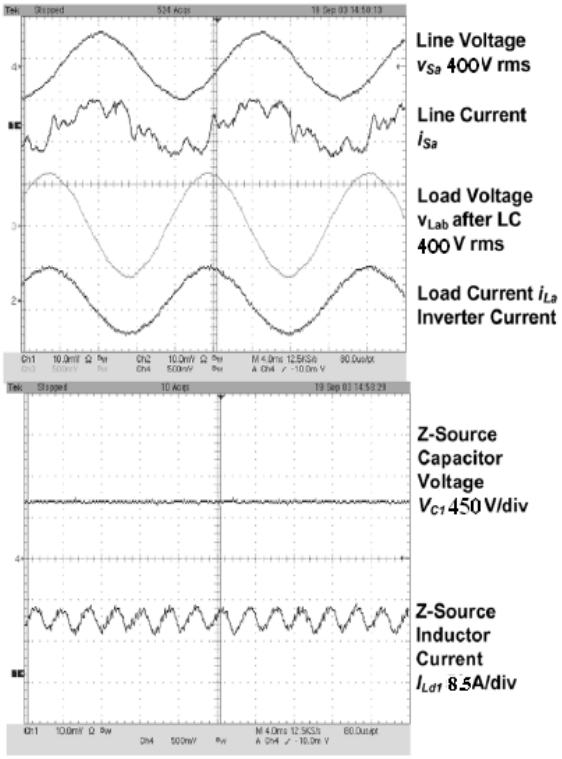

Fig. 14: Experimental waveforms under the nominal line voltage of 400 Vac

The inductor used in the Z-source has the similar effect on the line current harmonic reduction, which was confirmed in the above simulation results. For a motor drive system, the required dc capacitance is relatively small for a tolerable voltage ripple mainly resulted from rectification. The dc capacitance should be sized for possible regenerative operation. Figure 9 shows the current harmonic content in traditional inverters. Figure 10 shows the current harmonic content of Z source inverter which has better improvement when compared with traditional inverters.

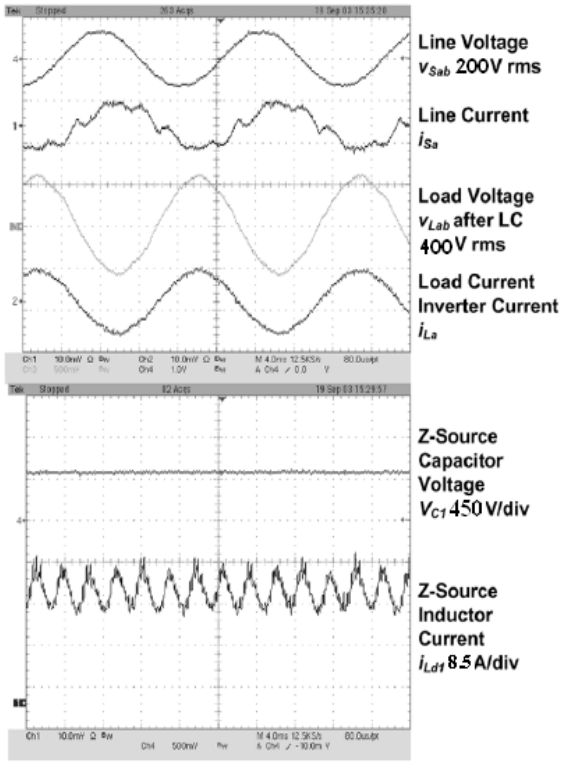

Fig. 15: Experimental waveforms under 50% voltage sag

Figure14 shows experimental waveforms under the nominal line voltage of 415-V rams. Again, the inverter produced a 400-V rms value, by boosting the dc capacitor voltage to 650 V. The dc voltage across the bridge was boosted to 650V with a boost factor of 1.21. Also, it can be seen that the line current contains much less harmonics than the traditional ASD without dc inductors, although the wave shape is different from the simulation. This is because the line voltage is distorted in the lab, which was not considered in the simulation. Figure 11 shows the voltage harmonic content in traditional inverters. Figure 12 shows the voltage harmonic content of Z source inverter which has better improvement when compared with traditional inverters. Figure 15 shows experimental waveforms during 50% voltage sag (the line voltage dropped to 200-Vrms), the same conditions as in the simulation Fig. 8.1 and 8.2. The waveforms clearly demonstrate hat the dc capacitor voltage can be boosted and maintained to a desired level, which is above 600V, It can be confirmed from the results that the boost factor was 2.8 and the modulation index was 0.82.

A prototype has been built to further verify the operation, theoretical relationships of voltage boost, and simulation results of the presented Z-source ASD system. Figure 13 shows a photo of the system. It should be noted that the inductors and capacitors were oversized in the prototype for possible regenerative operation during deceleration or inverter trips.

CONCLUSION

This paper has presented a new ASD system based on the Z-source inverter. The operating principle and analysis have been given the harmonic contents Simulation and experimental results verified the operational and demonstrated the promising features. In summary, the Z-source inverter ASD system has several unique advantages that are very desirable for many ASD applications,

* It can produce any desired output ac voltage, even greater than the line voltage
* Provides ride-through during voltage sags without any additional circuits and energy storage;
* Minimizes the motor ratings to deliver a required power;
* Reduces inrush and harmonic current.
* Unique drives features include buck-boost inversion by single power-conversion stage, improved reliability, strong EMI immunity, and low EMI
* The Impedance source technology can be applied to the entire spectrum of power conversion.

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