Design of a Low Cost IC Tester

[1]Liakot Ali, [1]Roslina Sidek, [1]Ishak Aris,
[2]Mohd. Alauddin Mohd. Ali and [1]Bambang Sunaryo Suparjo
[1]Department of Electrical and Electronic Engineering
Universiti Putra Malaysia, Serdang, Selangor, Malaysia
[2]Department of Electrical, Electronic and Systems Engineering
Universiti Kebangsaan Malaysia, Bangi, Selangor, Malaysia

Abstract: Low cost Integrated Circuit (IC) testing is now a burning issue in semiconductor technology. Conventional IC tester, Automatic Test Equipment (ATE), cannot cope with the today's continuously increasing complexities in IC technology. Deterministic algorithm, which is an idea of 1960's, is adopted in the ATE. Recently pseudo-random testing approach of IC testing has been emerged as an economically viable alternative to the expensive deterministic testing approach. This study introduces the design of a System-on-a-chip (Soc) implementing pseudo-random test technique for low cost IC testing with reliable performance. It is capable of testing combinational circuits as well as sequential circuits with scan-port facilities efficiently. It can also be used for testing Printed Circuit Board (PCB) interconnection faults.

Key words: ATE, seed, LFSR, SoC

INTRODUCTION

Dramatic improvement of integrated technology in IC manufacturing is rapidly leading to exceedingly complex, multi-million transistor chips. All the functionalities of an electronic system are being integrated on a single chip in less than 2 cm square silicon area. This growth is expected to continue full force for the future years. With the increase of such integration densities and complexities, problems associated with testing of ICs have become much more complex and acute[1]. The cost of testing has become a major portion of the total cost of an electronic product. It is predicted in a survey that it will soon cost more to test a transistor than to make it if current trends of increasing testing cost is maintained[2]. IC testing has now become a front-end issue in the semiconductor world, which needs an economic solution with reliable performance.

Modern IC manufacturing companies use ATE. The drawbacks of ATE are: (i) High equipment cost (ii) Slow test speed (iii) Huge memory requirements (iii) Tester inaccuracy. All the drawbacks of ATE are pointing towards having a new approach for cost effective IC testing. Otherwise all the benefits of semiconductor technology will be meaningless[3]. ATE is based on the deterministic algorithm. In deterministic approach[4], Circuit Under Test (CUT) is analyzed at the beginning of the test to generate pre-defined test patterns for detecting its faults. Deterministic test pattern enables error signals, generated due to presence of faults, and propagates them to some observable outputs from the faulty nodes or lines. This method guarantees full fault coverage but the increasing densities in the circuit lead to computational complexities and the requirements of huge amount of memory to store large test data volumes.

Pseudo-random approach[5] is now emerging as an economically viable alternative to the expensive deterministic testing. In this approach, a set of test vectors is generated randomly from 2^n possible input patterns (n= number of inputs). Linear Feedback Shift Registers (LFSRs) are commonly used for test pattern generation because it has a simple structure and can also be used as an output response analyzer. The main advantage of this approach is that the random pattern generation circuitry is simple and a large number of test pattern can be generated using smaller data storage.

The attempt to design and develop low cost IC tester has been prevalent among the researchers since 1970. A small tester was built in the laboratory d'Automatique de Grenoble in 1970 and performed some random testing trials[6]. Test processor chip based on weighted random test techniques have been reported[7]. This paper introduces the design of a SoC using pseudo-random test technique to develop a cost effective IC tester. The tester needs simpler hardware and control complexities and less memory space than that of others. The tester inaccuracy problem has also been addressed by introducing the concept of single chip IC tester which has been designed using industry standard HDL (hardware description language). In order to maintain the accuracy of the test, it is essential that the fabrication technology of the tester circuit should be at the leading edge with respect to the CUT. Since the design of the proposed SoC is in Verilog

HDL, which is technology independent, the soft core can be reused to new fabrication technology keeping pace with the today's continuously changing technology environment. The performance of the IC tester has been verified using the fault simulation technique. The following sections of this paper describe the design and operation of the SoC and performance verification of the SoC using fault simulation of benchmark circuits.

The design of the SoC: Figure 1 shows the functional block diagram of the SoC. Main modules of the SoC are a micro-UART (universal asynchronous receiver and transmitter), controller unit, test Pattern Generator (PG), Buffer Register (BR), Signature Analyzer (SA) and memory modules (RAMs). All the modules except memory modules are designed using Verilog HDL. The memory modules are used for the Altera Quartus library. Module by module design technique is used to design the SOC. Each functional module is designed and simulated and once its functionality is verified then another module is designed and verified using the same approach. Finally, all the modules of the SOC are integrated and simulated to verify its expected functionality in IC testing.

Description of the Modules:
Micro-UART: It consists of a transmitter and a receiver module. Data communication between a Personal Computer (PC) and the SoC is performed through the UART. It is named as micro-UART due to its modularity, configurability and extremely compact size[8]. A user friendly GUI as shown in the Fig. 2 has been developed using C++ Builder for key-in test information such as number of primary I/O, number of CUT scans-path, number of test set etc.
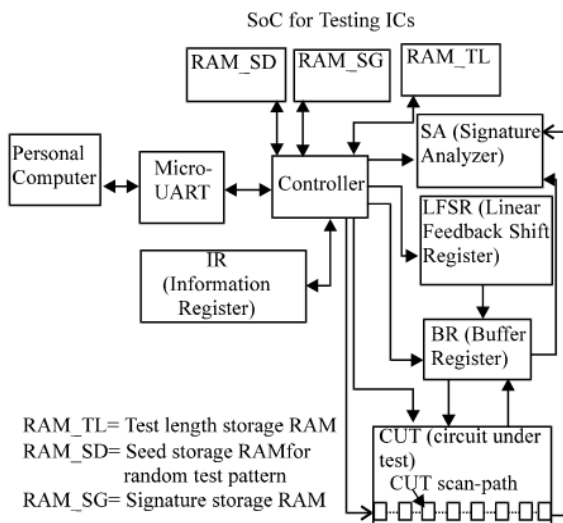
Controller: It consists of Finite State Machines (FSMs) and datapaths. FSMs generate sequence of necessary controlling pulses for loading data in the memory and executing the test process of the CUT.

Memory and Information Register (IR): Necessary information for testing CUT such as number of primary inputs, primary outputs, test set, test length etc. is stored in the IR and memory modules (RAMs). Three RAMs named as test length storage RAM (RAM_TL), seed storage RAM (RAM_SD) for random pattern generation and signature storage RAM (RAM_SG) have been used.

Pattern Generator (PG): It is a 32 bit LFSR and its feedback connection is according to primitive polynomial $P(X) = 1+X+X^{27}+X^{28}+X^{32}$.

Buffer Register (BR): The BR is also 32 bits. Test pattern generated from the PG is loaded into the BR and is applied to the CUT and the output response is also captured into the BR and is sent to the SA.
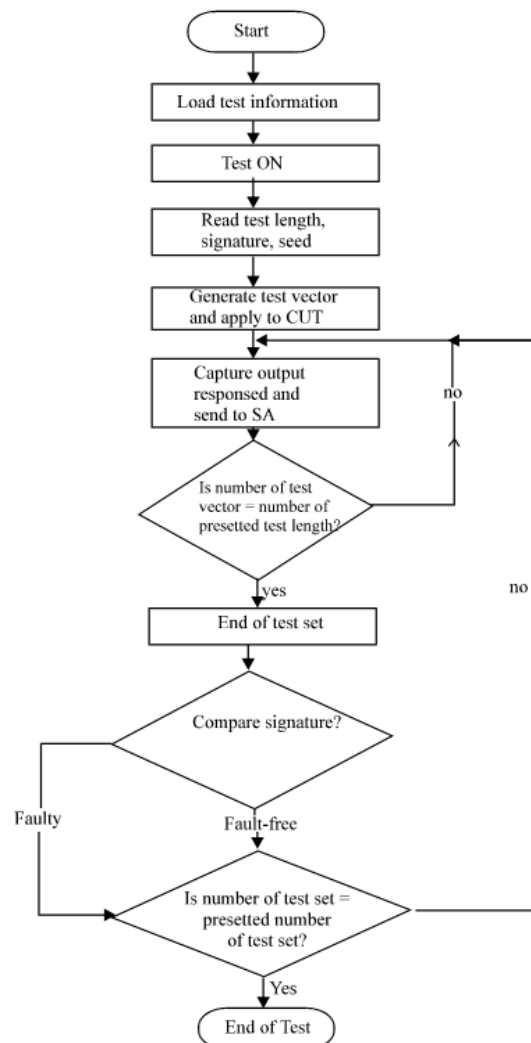

Fig. 1: Functional Block Diagram of the SoC

Fig. 2: Flowchart Showing the Test Process simulator

Signature Analyzer (SA): The SA has a similar structure of the PG except having two inputs. The state of the SA is given by the equation: $S(t+1) = [T].[s(t)]^T + [R(t)]^T$ where, $S(t+1)$ and $S(t)$ are SA states at times $t+1$ and t respectively. $[T]$ and $[R(t)]^T$ are the transition matrix of the SA and transpose of the response sequence of the CUT. Aliasing error of the SA is $1/2^{32}$.

Operation of the SoC: Operation of the SoC has two phases: (a) load/write data in the IR and the memory modules (b) circuit test and retrieval of test result.

Load/Write: Prior to IC testing, the following information is loaded in the IR and memory modules from the PC:

* Load the IR with necessary information such as number of CUT primary inputs and outputs, number of CUT scan paths, number of test sets,
* Load the test length of each test set in the test length storage RAM
* Load the data in the seed storage RAM for a random test pattern generation
* Load the reference signature in the signature storage RAM.

Circuit Test and Response Retrieval: At the beginning of the test of the IC, the PG, BR and SA are reset to zero and the test mode is set on from the GUI. The test sequences are as follows:

Loop1
  If test mode on {
  Read the test length of the 1st test set,

  Read the seed value of LFSR for the 1st test set,
  Read the reference signature for the 1st test set,
  Set seed in the LFSR by setting input set_seed=1,
  Loop2
  Enable LFSR for max (pi, Sp) clock cycles,
  Enable buffering register for max (pi, PO) clock cycles,
  Enable signature analyzer for max (pi, PO, Sp) clock cycles,
  Set the CUT to normal mode by setting input cnm=1 ;
    If cnm=1 {
      Apply test vector to the CUT
      Capture response and send to signature analyzer
      Increment test_counter value}
If test_counter value=presetted test length {
        End_set (e_set) =1 ;
        Compare   signature   with   the   reference signature }
Else Goto Loop2
If e_set=1 {
        Increment set_counter, }
If set counter_value=presetted number of test set {
        End_test (e_test) =1,

Ready for next test, }
}
Else Goto Loop 1

Specification of the SoC: Specifications of the SoC are as follows:

Maximum CUT input/output pins: 32
Maximum CUT scans-path: 128
Maximum test sets: 4
Maximum generated test vectors: 1.7×10^7
Maximum test length 2^{14} K

RESULTS

The design of the SoC has been compiled and simulated using the curtis EDA (Electronic design automation) tool. The proper logic level of the control signals in simulation results ensures the desired functionality of the SoC. To develop a prototype of the low cost IC tester, the design of the SoC has been released into physical hardware using APEX 20KE (part number EP20K200EFC484-2X) FPGA chip mounted on Nios development kit. A daughter test board has been designed to indicate the test results. A sample CUT (32-bit multiplier) has been tested using the prototype IC tester. A user-friendly GUI (graphical user interface) has been developed to load necessary test information into the IC tester. Test process can also be executed and test status can also be monitored using the GUI. Snap of the GUI and the hardware realization of the prototype IC tester are shown in Fig. 3 and 4, respectively.

For the evaluation of the performance of the IC tester, fault simulation experiments on ISCAS85 benchmark circuits[9] have been conducted using TetraMax fault of the Synopsis EDA tool. Pseudo-random testing approach has the drawbacks of requirements of higher number of test vectors to achieve acceptable fault coverage. This problem has been overcome by using appropriate seed of the LFSR. Summary of the fault simulation results has been presented in the Table 1.
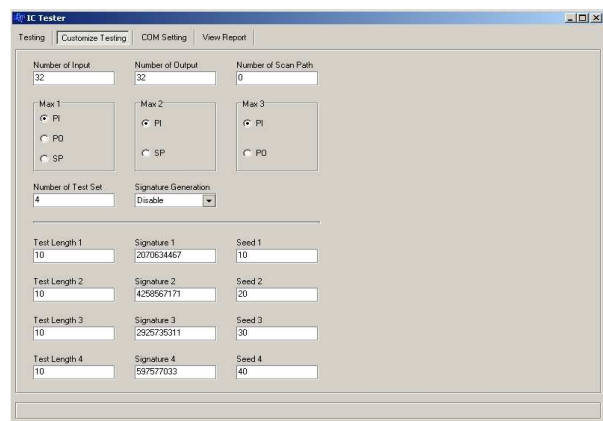

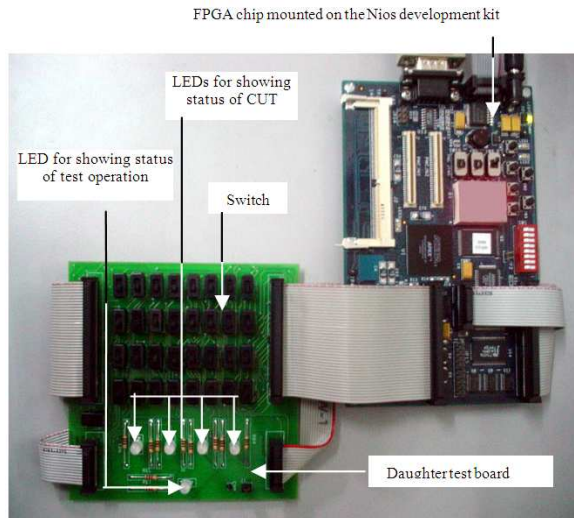Fig. 3: Graphical User Interface between the SoC and the PC

Fig. 4: Prototype of the LOW Cost IC Tester

Table 1: Summary of the Fault Simulation Results

ISCAS85 Benchmark circuits	Number of test vector	% Fault coverage
C432	288	100
C499	928	100
C880	384	98.74
C1355	1300	100
C1908	2208	100
C5315	1408	99.13
C6288	128	100

The Table 1 shows that if the LFSR is initialized using appropriate seed then it is capable of producing acceptable fault coverage using a lower number of test vectors. The results are comparable with that of other researchers[7, 10].

CONCLUSION

Design of a cost effective IC tester has been presented. Since the IC tester is SoC, it posses improved performance, improved reliability, reduced power consumption, reduced cost, reduced system size and short time-to-market. It requires lower data storage requirements. The performance of the tester has been verified using fault simulation experiments on ISCAS85 benchmark circuits which shows that it is capable of producing 100% fault coverage using a lower number of test vectors.

ACKNOWLEDGMENT

REFERENCES

1. Liakot, A., S. Roslina, A. Ishak, M.A. Alauddin and S.S. Bambang, 2004. Challenges and directions for IC testing. Integration, the VLSI J., 37: 17-28.
2. Needham, W.M., 1999. Nanometer technology challenges for test and test equipment. Computer, 32: 52-57.
3. Agrawal, V.D. and C.S. Sharad, 1988. Test Generation for VLSI Chips. Comp. Society Press, Washington.
4. Hamzaoglu, I. and J.H. Patel, 1998. New techniques for deterministic test pattern generation. 16th IEEE Proceedings of VLSI Test Symposium, pp: 446-452.
5. Bardell, P.H., W.H. McAnney and J. Savir, 1987. Built-in Test for VLSI: Pseudorandom Techniques. John Wiley and Sons, New York, USA.
6. David, R., 1998. Random Testing of Digital Circuits: Theory and Applications. Marcel Dekker Inc., New York.
7. Iftekhar, A., 1995. VLSI circuit testing using a probabilistic approach. Ph.D. Thesis, Universiti Kebangsaan Malaysia.
8. Liakot, A., S. Roslina, A. Ishak, M.A. Alauddin and S.S. Bambang, 2004. Design of a Micro-UART for SoC application. Intl. J. Comp. and Elect. Eng., 30: 257-268
9. Braglez, F. and H. Fuziwara, 1985. A neural netlist of 10 combinational bench-mark circuits and target translator in FORTRAN. Special Session on ATPG and Fault Simulation, International Symposium on Circuits and Systems, Kyoto, Japan.
10. Wunderlich, H.J., 1990. Multiple distributions for biased random test patterns. IEEE Trans. On Comp. Aided Design, 9: 584-593.