

DFM of Strained-Engineered MOSFETs Using Technology CAD

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Abstract: Problem statement: In this study, a systematic study based on Technology CAD (TCAD) was taken up for the design and Virtual Wafer Fabrication (VWF) of strain-engineered MOSFETs in Si CMOS technology. **Approach:** A simple manufacturable process recipe was developed to induce uniaxial stress in channel region to obtain enhanced performance in CMOS in 45 nm technology node. **Results:** Using Synopsys Sentaurus Process simulation tool, high dopant activation and low Transient Enhanced Diffusion (TED) during processing are fully captured. A physics-based mobility model had been developed and implemented in Synopsys Sentaurus Device tool. Sentaurus Device was used to simulate device DC and AC characteristics and also to extract V_{th} , I_{on} and I_{off} . **Conclusion:** Optimum process conditions required to meet a set of device specifications had been achieved via the Design of Experiment (DoE) study. Process Compact Model (PCM) was used for performance and manufacturability optimization.

Key words: Technology CAD, process compact model, strained-engineered MOSFETs

INTRODUCTION

As MOSFET device dimensions approach their physical limits (Maiti *et al.*, 2007a), TCAD tools that can accurately simulate IC fabrication process technology and device characteristics are indispensable for advanced technology development and manufacturing. TCAD is now an integral part of Integrated Circuit (IC) manufacturing due to its predictive capability for the process, device and circuit simulations. TCAD has also the power to analyze accurately the impact of process parameter variations on device characteristics and may be used to address and control process variability as needed for modeling the semiconductor manufacturing process. During process modeling, generally a systematic Design of Experiments (DoE) run is performed. DoE can be systematically set up, with control over process parameters and arbitrary choice of device performance characteristics. The models developed from DoE are known as Process Compact Models (PCMs). They are analogous to compact models for semiconductor devices and circuits. PCM may be used to capture the nonlinear behavior and multi-parameter interactions in manufacturing processes.

In this study, we report on a systematic TCAD-based study towards design and optimization of strain-

engineered MOSFETs in 45 nm technology node using Sentaurus TCAD tools (Synopsys, 2008a; 2008b). Sentaurus Process simulator have been used to perform process simulation. The development of the process-strain induced mobility model and its implementation in Sentaurus Device simulator have been described. The simulated DC and RF characteristics for Process-induced Strained-Si (PSS) p- and n-MOSFETs and a comparison with the reported experimental results are presented. We have also presented the results of the PCM studies via the variation of technological parameters for the optimization of strain-engineered MOSFETs.

In previous study (Abdallah and Nabhan, 2009), a switched-capacitor filter with a high stop band attenuation and low passband ripple is proposed and analyzed. Graphic-based simulation model of the DSSC is presented in PSCAD/EMTDC and using this model a harmonic analysis is carried out to define (Fajri *et al.*, 2008).

The earlier study will reduce procedure of CT scanning and design time for patients with not very large or complex defect (Sena and Piyasin, 2008). Design of standardized skull implants therefore will help the surgeon in implant preparation, by selecting implant that matches well with each case.

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MATERIALS AND METHODS

Sentaurus Process tool is used to simulate and optimize a typical 45 nm process flow, including channel, halo, Source/Drain (S/D) engineering, oxidation, deposition, etching and annealing for dopant activation. The stress history is calculated for the entire process flow. Strain sources are lattice mismatch (SiGe pocket) for PSS p-MOSFETs and intrinsic stress (compressive cap) for PSS n-MOSFETs. Source/drain SiGe pocket is formed with 17% Ge at room temperature and nitride cap layers are introduced after the critical doping steps and, therefore, have negligible impact on the final doping distributions. A three-stream diffusion model is used. Additionally, formation of point-defect clusters and the three phase segregation model account for the dose loss at the silicon-oxide interface are considered. For simulation of ion implantation, a 2D analytic integration with dual Pearson (in silicon) and Pearson primary distribution functions (in other materials) is used. For the simulation of Ge diffusion and redistribution in strained-Si a model is used which supports structures with various regions containing strained-Si. At each diffusion step, the stress evolution is computed including oxidation steps based on the viscoelastic model. The strain calculation also includes the compression due to Ge incorporation. The $Si_{0.83}Ge_{0.17}$ pockets induce uniaxial compressive stress in different areas of the structure, including the channel. This may be seen in the stress distribution after S/D anneal as presented in Fig. 1a. The nitride film transfers the stress to the channel because an edge force is developed as the film grows over the spacer and the gate. Figure 1b shows the device structure simulated with highly tensile cap layer and tensile stress in the channel area. The structure generated by Sentaurus Process is then simulated using Sentaurus Device. The simulated device performance includes: DC electrostatic behavior with strain-induced mobility enhancement and the impact of Rapid Thermal Annealing (RTA) on device performance. Table 1 shows the major process parameters used in simulation. Hydrodynamic transport model was used in device simulations.

Strain-induced mobility model: In developing the strain-induced mobility model, we implemented strain effects by considering scattering of mobile charges in process-induced strained-Si n- and p-MOSFETs due to electron/hole-phonon interactions in strained-Si channel. To obtain the strained induced mobility, first we calculated strain-induced interaction potential scattering by acoustic phonon. Then we use Fermi's golden rule to obtain the electron/hole-phonon scattering rates. Towards this, one needs to obtain the matrix element for electron-phonon scattering. The matrix element describes the coupling between initial

and final electronic states due to interactions with scattering charge centers. Finally, we integrate the matrix elements over all final states to obtain the scattering rate between electron/hole-phonon.

Strain-induced interaction potential scattering by acoustic phonon: In a deformed Si substrate the coordinates of its lattice point are displaced. If the radius vector of a lattice point in undeformed condition is r and in deformed condition is r' , then the displacement vector is given by:

$$u(r) = r' - r \tag{1}$$

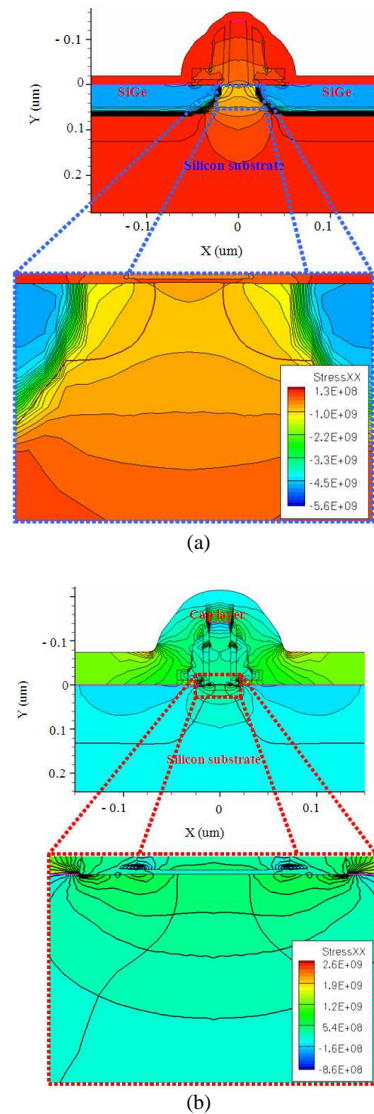


Fig. 1: 2-dimensional device structures of 45 nm MOSFETs obtained from Sentaurus Process simulation (a) p-MOSFET and (b) n-MOSFET

Table 1: Major technology parameters considered in TCAD simulation for the virtual fabrication of process-induced strained-Si MOSFETs

Parameter	PSS p-MOSFET	PSS n-MOSFET
Channel implants	P, 370 KeV, 2.65e13 cm ⁻²	B, 300 KeV, 3.0e13 cm ⁻²
Well	P, 260 KeV, 2.65e13 cm ⁻²	B, 120 KeV, 2.05e13 cm ⁻²
	P, 40 KeV, 1.0e13 cm ⁻²	B, 50 KeV, 1.1e13 cm ⁻²
V _{th} adjustment	B, 150 KeV, 1.0e13 cm ⁻²	B, 25 KeV, 1.0e13 cm ⁻²
Poly doping	BF2, 10 KeV, 2.1e15 cm ⁻²	P, 10 KeV, 2.1e15 cm ⁻²
Halo implants	As, 20 KeV, 5.0e13 cm ⁻²	B, 10 KeV, 6.0e13 cm ⁻²
Source/Drain Extension (SDE)	B, 1.0 KeV, 1.0e14 cm ⁻²	As, 5.0 KeV, 8.0e14 cm ⁻²
Deep source/Drain (HDD)	B, 5.0 KeV, 1.0e15 cm ⁻²	P, 15 KeV, 1.5e15 cm ⁻²
Final RTA	1025°C, 1.0 sec	1025°C, 1.0 sec

The deformation may be described in terms of symmetrical strain tensor as:

$$u_{im} = \frac{1}{2} \left(\frac{\partial u_i}{\partial x_m} + \frac{\partial u_m}{\partial x_i} \right) = u_{mi} = u^i \delta_{im} \quad (2)$$

If the distance between two lattice points of an undeformed Si substrate is dl, of the deformed Si substrate (strained-Si substrate) is dl', then we get:

$$dl^2 = dx^2 + dy^2 + dz^2 = \sum_{i=1}^3 dx_i^2 \quad (3)$$

and:

$$\begin{aligned} dl'^2 &= \sum_{i=1}^3 dx_i'^2 = \sum_{i=1}^3 (dx_i + du_i)^2 \\ &= \sum_{i=1}^3 (dx_i^2 + 2dx_i du_i + du_i^2) \end{aligned} \quad (4)$$

The tensor du_i determines the variation of distances between the lattice points. Neglecting the quantity du_i² and expressing du_i in terms dx_m:

$$du_i = \sum_{m=1}^3 \frac{\partial u_i}{\partial x_m} dx_m \quad (5)$$

and combining Eq. 3-5 we obtain dl'² as:

$$dl'^2 = \sum_{i=1}^3 dx_i'^2 = dl^2 + 2 \sum_{i,m=1}^3 \frac{\partial u_i}{\partial x_m} dx_i dx_m \quad (6)$$

Taking into account Eq. 2 we obtain for dl'²:

$$\begin{aligned} dl'^2 &= dl^2 + \sum_{i,m=1}^3 \left(\frac{\partial u_i}{\partial x_m} + \frac{\partial u_m}{\partial x_i} \right) dx_i dx_m = dl^2 \\ &+ 2 \sum_{i,m} u_{im} dx_i dx_m \end{aligned} \quad (7)$$

We may write from Eq. 7:

$$dl' = \sqrt{dl^2 + 2 \sum_{i,m} u^i \delta_{im} dx_i dx_m} = \sqrt{dl^2 + 2 \sum_i u^i dx_i^2} \quad (8)$$

The variation of volume upon deformation is given by:

$$\begin{aligned} \Delta V' &= dx' dy' dz' = dx (1 + u^{(1)}) dy (1 + u^{(2)}) dz (1 + u^{(3)}) \\ &= \Delta V (1 + u^{(1)} + u^{(2)} + u^{(3)}) \end{aligned} \quad (9)$$

Therefore the local dilation Δr is given by:

$$\Delta(r) = \frac{\Delta V' - \Delta V}{\Delta V} = \sum_i u^{(i)} = \sum_i u_{ii} = \sum_i \frac{\partial u_i}{\partial x_i} = \nabla \cdot u(r) \quad (10)$$

Above local dilation is equivalent to displacement of the atoms and hence equivalent to a local change of lattice parameter. Therefore, it induces a modification of both the bands: (a) valance band (E_C) and (b) valance band (E_V). The interaction potential H_{e-ph}^{AC} of the acoustic phonon with the lattice depends on the variation of conduction band and valance band edge. Since phonons deform the crystal in three dimensions, we can assume for small stress and for an isotropic crystal, interaction potential is given by:

$$H_{e-ph}^{AC} = \Xi \frac{\delta V}{V} = \Xi \nabla \cdot u(r) \quad (11)$$

where, Ξ is the so-called deformation potential. The lattice displacement u(r) for long wavelength phonon is given by (Kittel, 1987):

$$\bar{u}(r) = \sum_q \bar{w}_q \left(\frac{\hbar}{2\rho\omega_q} \right)^{1/2} \left(a_q e^{(iq \cdot r)} + a_q^\dagger e^{(-iq \cdot r)} \right) \quad (12)$$

Where:

ρ = The semiconductor density

\bar{w}_q = The polarization vector

For longitudinal phonons, the polarization vector is $\bar{w}_q = \frac{\bar{q}}{q} = \hat{q}$. Thus the acoustic deformation potential may be written as:

$$H_{e-ph}^{AC} = \Xi \frac{\delta V}{V} = \Xi \nabla \cdot \bar{u}(\vec{r}) = i \sum_q (\bar{w}_q \cdot \bar{q}) \left(\frac{\hbar \Xi^2}{2\rho\omega_q} \right)^{1/2} \left(a_q e^{i\bar{q}\cdot\vec{r}} - a_q^\dagger e^{-i\bar{q}\cdot\vec{r}} \right) \quad (13)$$

Transition probability for acoustic phonon scattering: The scattering rate of electrons or holes by lattice vibration in presence of strain may be explained in terms of the corpuscular model with the aid of phonon concept. Charge carriers colliding with phonons exchange energy and quasi-momentum with it. Since the number of phonon depends on temperature, the charge scattering should be temperature dependent. However, in order to calculate the quantum transitions of electrons and holes from state to state, the perturbation generated by deformation potential due to strain should be applied. Once we have the acoustic deformation potential, one may obtain the scattering rate using Fermi's golden rule:

$$\Gamma_{i \rightarrow f} = \frac{2\pi}{\hbar} \left| \langle f | H_{e-ph}^{AC} | i \rangle \right|^2 \delta(E_f - E_i) \quad (14)$$

where, f and i refer to final and initial states. The energy of lattice vibrations under electrons or holes phonon interaction may change by the creation or annihilation of phonon. Hence, in collisions the initial and the final energies of the electron/hole-phonon system are:

$$\left. \begin{aligned} E_i &= E_k + n_q \hbar\omega_q \\ E_f &= E_{k'} + n'_q \hbar\omega_q \end{aligned} \right\} n'_q = n_q \pm 1 \quad (15)$$

Hence, transition probability for the state E_k to $E_{k'}$ in an electron/hole phonon collision involves phonon in the wave vector q is:

$$\Gamma_{k \rightarrow k'} = \frac{2\pi}{\hbar} \left| \langle k' | H_{e-ph}^{AC} | k \rangle \right|^2 \delta(E_k - E_{k'} \pm \hbar\omega_q) \quad (16)$$

Strain-induced scattering matrix: If $\psi_k(\vec{r})$ is the eigenfunction for the unstrained condition and $\psi_k(\vec{r}, \epsilon)$ is the eigenfunction for strained condition, then:

$$\psi(\vec{r}, \epsilon) = u_k(\vec{r}, \epsilon) e^{i\vec{k}\cdot\vec{r}} = \psi(\vec{r}) + \delta\psi(\vec{r}) \quad (17)$$

Now the scattering matrix elements for long wavelength acoustic phonon scattering in isotropic material are given as (Roblin and Rohdin, 2001):

$$\mathfrak{S}(k', k) = \langle k' | H_{e-ph}^{AC} | k \rangle = i \sum_q (\bar{w}_q \cdot \bar{q}) \left(\frac{\hbar \Xi^2}{2\rho\omega_q} \right)^{1/2} \int \left[\psi_{k'}^* \phi_{n'_q}^* (a_q e^{i\bar{q}\cdot\vec{r}} - a_q^\dagger e^{-i\bar{q}\cdot\vec{r}}) \psi_k \phi_{n_q} dV \right] \quad (18)$$

Now, considering:

$$\psi_k = u_k(\vec{r}) e^{i\vec{k}\cdot\vec{r}}, \quad \psi_{k'} = u_{k'}(\vec{r}) e^{-i\vec{k}'\cdot\vec{r}} \quad (19)$$

$$a_q \phi_{n_q} = \sqrt{n_q} \phi_{n_q-1}, \quad a_q^\dagger \phi_{n_q} = \sqrt{(n_q+1)} \phi_{n_q+1} \quad (20)$$

Where:

a_q^\dagger and a_q = The creation and annihilation operator

ψ_k and ϕ_q = The wave function of the electron and lattice vibration mode of vector \bar{q}

Now substituting Eq. 19 and 20 in 18, one obtains:

$$\mathfrak{S}(k', k) = i \sum_q (\bar{w}_q \cdot \bar{q}) \left(\frac{\hbar \Xi^2}{2\rho\omega_q} \right)^{1/2} \int \left[\frac{u_{k'}^* \phi_{n'_q}^* u_k \phi_{n_q-1} \sqrt{n_q} e^{i(\vec{k}+\bar{q}-\vec{k}')\cdot\vec{r}} - u_{k'}^* \phi_{n'_q}^* u_k \phi_{n_q+1} \sqrt{n_q+1} e^{i(\vec{k}-\bar{q}-\vec{k}')\cdot\vec{r}}}{\sqrt{n_q+1} e^{i(\vec{k}-\bar{q}-\vec{k}')\cdot\vec{r}}} \right] dV \quad (21)$$

Relaxation time for acoustic phonon scattering: The well known equation to define relaxation time is given by (Nag, 2001):

$$\frac{1}{\tau} = \frac{V}{(2\pi)^3} \int \left(1 - \frac{k' \cos \theta'}{k \cos \theta} \right) \Gamma_{k \rightarrow k'} dk' \quad (22)$$

Replacing and combining Eq. 16, 18 and 22 we get the following expression as:

$$\frac{1}{\tau} = \frac{1}{(2\pi)^3} \left(\frac{\pi \Xi^2}{\rho} \right) \int \left[\frac{(n_q+1)}{\omega_q} q^2 \delta(E_{k'} - E_k + \hbar\omega_q) + \frac{n_q}{\omega_q} q^2 \delta(E_{k'} - E_k - \hbar\omega_q) \right] \left(1 - \frac{k' \cos \theta'}{k \cos \theta} \right) dk' \quad (23)$$

where, n_q represents the occupation number of acoustic phonons with wave vector \bar{q} . Since an electron or hole

may change its state from k by emission or absorption of an acoustic phonon of energy $\hbar\omega_q$, there are two terms involved in $\Gamma_{k \rightarrow k'}$ corresponding to these two types of transitions. Since $\vec{k}' = \vec{k} + \vec{q}$, the integral may be also carried out in q -space. τ may therefore, be written as:

$$\frac{1}{\tau} = \frac{1}{(2\pi)^3} \left(\frac{\pi \Xi^2}{\rho} \right) \int \left[(n_q + 1) \delta(E_{k'} - E_k + \hbar\omega_q) + n_q \delta(E_{k'} - E_k - \hbar\omega_q) \right] \frac{q^2}{\omega_q} \left(1 - \frac{k' \cos \theta'}{k \cos \theta} \right) d\vec{q} \quad (24)$$

The element of volume $d\vec{q}$ in q -space may be expressed in spherical coordinate system as:

$$d\vec{q} = q^2 \sin \beta d\beta d\phi d\alpha \quad (25)$$

For the sake of convenience the direction of \vec{k} is taken as the polar axis and the azimuthal angle ϕ is measured with reference to plane containing the direction of the field and the vector \vec{k} as shown in Fig. 2. Thus we get:

$$\frac{1}{\tau} = \frac{1}{(2\pi)^3} \left(\frac{\pi \Xi^2}{\rho} \right) \int_{q_{\min}}^{q_{\max}} \int_0^{2\pi} \int_0^\pi \left[(n_q + 1) \delta(E_{k'} - E_k + \hbar\omega_q) + n_q \delta(E_{k'} - E_k - \hbar\omega_q) \right] \frac{q^2}{\omega_q} \left(1 - \frac{k' \cos \theta'}{k \cos \theta} \right) q^2 d\alpha d\beta d\phi \quad (26)$$

For the uniaxial strain-induced transformation of the isoenergetic surface, the deformed spheres transform into the oblate ellipsoid in the heavy-hole band and elongated ellipsoid in the light holes band (Kolomoets *et al.*, 2009). For this case Ξ is function of β , i.e., $\Xi(\beta)$ and:

$$\delta(E_{k'} - E_k \mp \hbar\omega_q) = \delta \left(\frac{\hbar^2 k'^2}{2m^*} - \frac{\hbar^2 k^2}{2m^*} \mp \hbar v q \right) = \delta \left(\frac{\hbar^2 k^2}{2m^*} \pm \hbar v q \cos \theta \mp \hbar v q \right) \quad (27)$$

For the azimuthal average approximation we can take $\omega_q = vq$ where v , is velocity of the mode averaged over direction. Regarding n_q , a simple case is considered and most commonly applicable is the case of equipartition and is given by:

$$n_q = \frac{1}{e^{\hbar\omega_q/k_B T} - 1} \approx \frac{k_B T}{\hbar\omega_q} \quad \frac{k_B T}{\hbar\omega_q} \ll 1 \quad (28)$$

Since there is energy and momentum conservation limit, we take $q_{\min} = 0$ to $q_{\max} = 2k$, a typical phonon energy is $\hbar vk$. When $n_q \gg 1$, the rates for absorption and emission become almost identical. Substituting Eq. 27 and 28 in 26 and using above approximations for a spherical band, one obtains:

$$\frac{1}{\tau} = \frac{k_B T}{8\pi^2 \hbar \rho v^2} \int_{q_{\min}}^{q_{\max}} \int_0^{2\pi} \int_0^\pi \Xi^2(\beta) (E_{k'} - E_k \mp \hbar\omega_q) q^2 d\alpha d\beta d\phi \quad (29)$$

However, semiconductors having ellipsoidal constant energy surfaces (for uniaxial strain), the matrix element for the acoustic phonon scattering is not isotropic. It is found that the relaxation time for this case may be expressed in two components, one perpendicular to the axis of symmetry of band structure and the other parallel to it. Using the relation $\rho v^2 = S_{ij}$, where S_{ij} is the elasticity constant modulus, the components may be expressed as:

$$\left. \begin{aligned} \frac{1}{\tau_{\parallel}} &= \frac{3\pi m_D^{3/2}}{S_{ii}} \frac{k T E_k^{1/2}}{2^{3/2} \pi^2 \hbar^4} (\xi_{\parallel} \Xi_d^2 + \eta_{\parallel} \Xi_d \Xi_u + \zeta_{\parallel} \Xi_u^2) \\ \frac{1}{\tau_{\perp}} &= \frac{3\pi m_D^{3/2}}{S_{ii}} \frac{k T E_k^{1/2}}{2^{3/2} \pi^2 \hbar^4} (\xi_{\perp} \Xi_d^2 + \eta_{\perp} \Xi_d \Xi_u + \zeta_{\perp} \Xi_u^2) \end{aligned} \right\} \quad (30)$$

where, S_{ii} now represents an average elastic constant for longitudinal waves, $\xi_{\parallel}, \eta_{\parallel}, \zeta_{\parallel}, \xi_{\perp}, \eta_{\perp}$ and ζ_{\perp} , are dimensionless constant, Ξ_d is the deformation potential constant for dilation and Ξ_u that for uniaxial strain. M_D is the density of states effective mass for ellipsoidal energy surface.

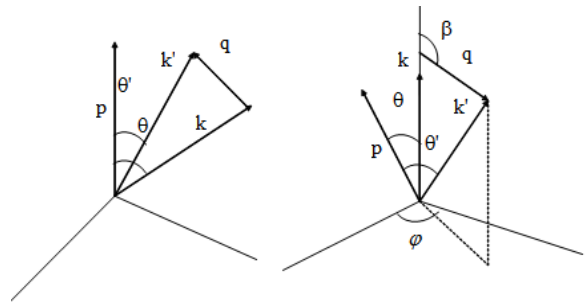


Fig. 2: Reference coordinate system

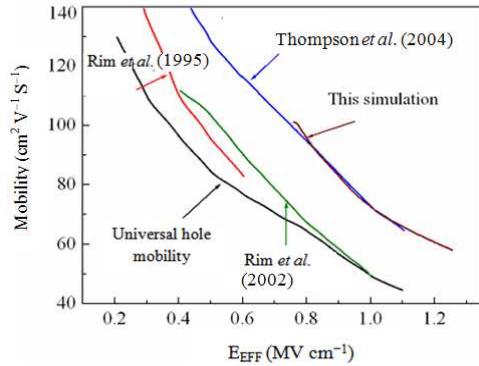


Fig. 3: Computed strained-Si hole mobility Vs vertical electric field

Implementation of mobility model: Elasticity modulus S_{ij} [10^{12} dyn cm^{-2}] is specified in the field $S_{[ij]}$ in the parameter file in the device simulator. The values of S_{11} , S_{12} and S_{44} are 1.23×10^{12} , -4.76×10^{12} and 0.8×10^{12} respectively (Synopsys, 2008b). Total deformation potential constant (Ξ) for conduction and valance bands were taken as 9.5 and 6.6 eV, respectively (Sun *et al.*, 2007). For the case with 500 MPa uniaxially compressive stress in Si, E_k was assumed to be 25 meV. Scattering by neutral centre, scattering by impurity ion were also considered in simulation. As all the mechanisms are independent of each other, the total scattering probability is equal to the sum of probabilities of scattering by scattering centers of all types. Hence, the mobility model is given by:

$$\mu_r = \langle \tau \rangle = \frac{e \langle \tau \rangle}{m_D^*} = \frac{e}{m_D^*} \left\langle \frac{1}{\sum \tau_i(E)} \right\rangle \quad (31)$$

The above mobility was considered in hydrodynamic model and was implemented in the Sentaurus Device simulator. To activate the mobility model, appropriate mobility values were defined in the fields of the parameter file of the device simulator. The simulated hole mobility Vs. electric field for process-induced strained-Si p-MOSFET is shown in Fig. 3. Our simulation data for the drain current (I_{ds}) Vs gate voltage (V_{gs}) have also been calibrated against reported experimental data (Ghani *et al.*, 2003).

RESULTS AND DISCUSSION

In this study, the impact of a strained-Si channel on device performance is evaluated in Sentaurus Device in which the mobility model has been incorporated.

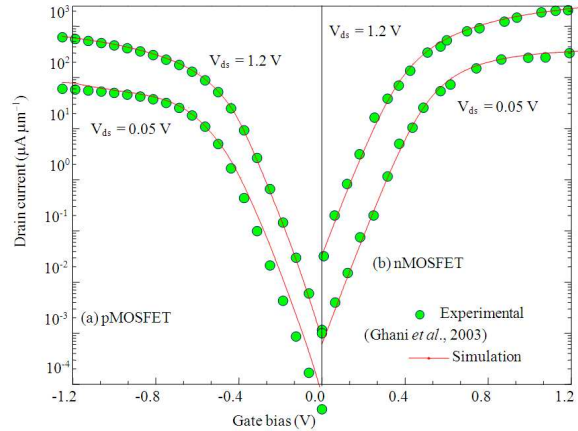


Fig. 4: Calibration of simulated I_d - V_g characteristics with reported experimental device data (Ghani *et al.*, 2003)

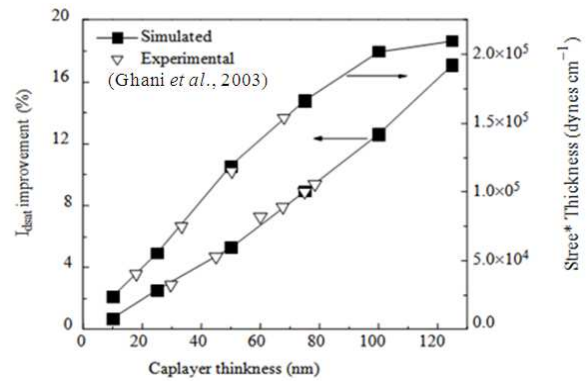


Fig. 5: Comparison of simulated and experimental (Ghani *et al.*, 2003) integrated film stress and resultant I_{Dsat} improvement as a function of film thickness

The MOSFET structures with embedded-SiGe (e-SiGe) Source/Drain layers for p-MOSFETs and a highly tensile silicon-nitride cap layer for n-MOSFETs used in simulation were chosen from the reference (Ghani *et al.*, 2003) as reliable experimental data are available for benchmarking and validating the predictive simulation results. Briefly, the MOSFETs have a gate length of 45 nm with 1.2 nm gate oxide. Experimental data were reported for two different drain biases and the measured drain current vs. gate voltage is shown Fig. 4 along with our simulation results. A good agreement is observed showing the prediction capability of TCAD simulation. Figure 5 shows a comparison between simulated and measured integrated film stress and the resultant process-induced strained-Si n-MOSFETs drain current (I_{dsat}) improvement as a function of film thickness.

Figure 6 shows the I_d - V_{ds} characteristics of the 45 nm MOSFETs with and without strained-Si channel. For the n-MOSFETs, the simulated results indicate an approximately 23% increase in drain current at $V_{ds} = V_{gs} = 1.2$ V due to an enhancement in electron mobility as a result of the strain in the channel. An empirical relationship between the strain components and the linear drain current has been reported in reference (Maiti *et al.*, 2007b). The change in linear drain current for p-MOSFETs may be expressed as (Yeo *et al.*, 2004):

$$\frac{\Delta I_{dlin}}{I_{dlin}} = a_x \epsilon_{xx} + a_y \epsilon_{yy} + a_z \epsilon_{zz} \quad (32)$$

where, a_x , a_y and a_z are the strain sensitivity coefficients with respect to the x, y and z strain components, respectively. Since $\Delta I_{dlin}/I_{dlin} \approx \Delta \mu/\mu$, the mobility enhancement is approximately the same as the linear drain current enhancement. Using the Eq. 32, we have computed the electron and hole mobility enhancement factor due to tensile and compressive longitudinal stress for strain-engineered n- or p-MOSFETs, respectively.

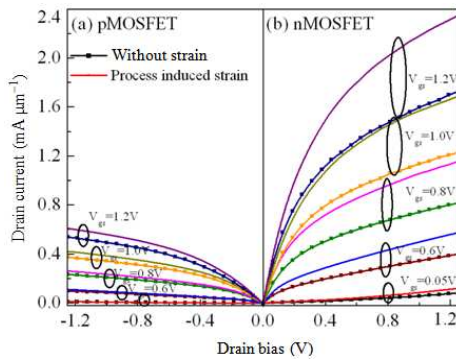


Fig. 6: Simulated I_d - V_d characteristics with different drain bias

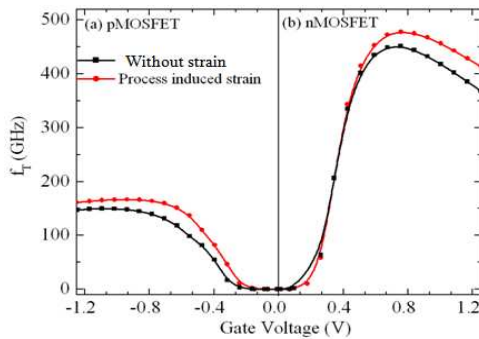


Fig. 7: Cut-off frequency (f_T) as a function of gate bias for 45 nm process-induced strained-Si p- and n-MOSFETs

For the PSS p- and n-MOSFETs hole and electron mobility enhancement factor have been found to be $\sim 1.5x$ and $\sim 1.8x$ than that of bulk-Si, which is also consistent with our simulation results. The resulting simulation demonstrates an approximately 17% enhancement in drain current with respect to the bulk-Si p-MOSFETs. An AC simulation is performed at equidistant bias points from small-signal AC analysis at various frequencies, with the gate as the input port, the drain as the output port and the source and substrate grounded. The resulting small-signal admittance and capacitance parameters are then used to extract RF Fig. 7 of merit, such as the cut-off frequency (f_T). The bias dependence of f_T is shown in Fig. 7.

Process optimization for strain-engineered MOSFETs using process compact model: Process variability has become a primary concern with regard to manufacturability and yield. As device dimensions shrink, the sensitivity of device performance to process variation also increases. With 45 nm processes, it is imperative to develop a systematic TCAD-based methodology to design, characterize and optimize manufacturability to increase yield (Montgomery, 2000).

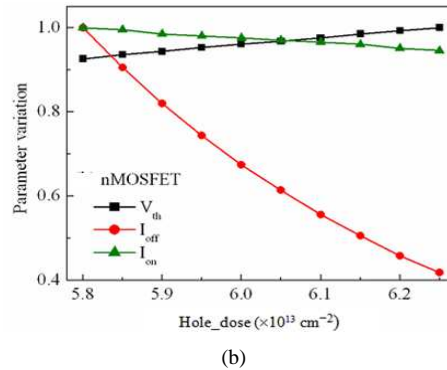
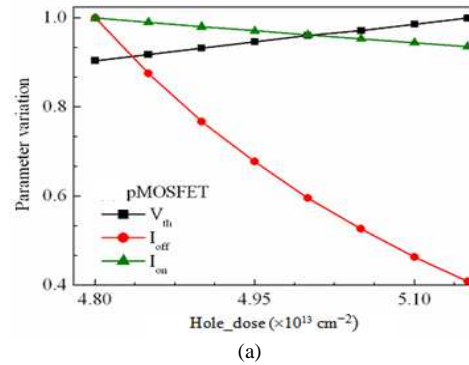


Fig. 8: Sensitivity response of (a) p- and (b) n-MOSFET with respect to halo implant dose

As the manufacturability of a process technology may be evaluated by the process window, defined as the area between the lower and upper limits of the critical process variables that yields acceptable device performance, in the following, we use the Sentaurus Process Compact Model (PCM) studio for the strain-engineered MOSFETs.

For the determination of the influence of tolerances in the technology process optimization different process parameters have been varied. Before running the systematic TCAD simulations, a sensitivity analysis is performed to determine the critical process variables and suitable ranges for the experimental design. Figure 8a and b illustrate the sensitivity of the p- and n-MOSFET responses with respect to the halo implant dose, respectively. Figure 9 shows a normalized histogram plot summarizing the sensitivity analysis for the critical process steps.

To demonstrate process optimization using PCM studio, one device parameter, e.g., threshold voltage (V_t) is chosen and the process is optimized with respect to V_t . As an example, we optimize the device performance by minimizing threshold Voltage (V_t) which mainly depends on the following parameters; Halo implant Dose (Halo_Dose) and Extension implant Dose (Ext_Dose), gate length (L_g); gate oxide thickness(G_{ox}), peak temperature for Rapid Thermal Annealing (RTA) which modifies the doping concentration in the channel region. The optimization problem consists of finding the best combination of the above parameters that produces the desired threshold voltage. The visual optimization procedure allows one to put constraints on the input parameters which however, are motivated by the manufacturing considerations. For an example, we may set a minimum for the gate length to obtain a nominal threshold voltage.

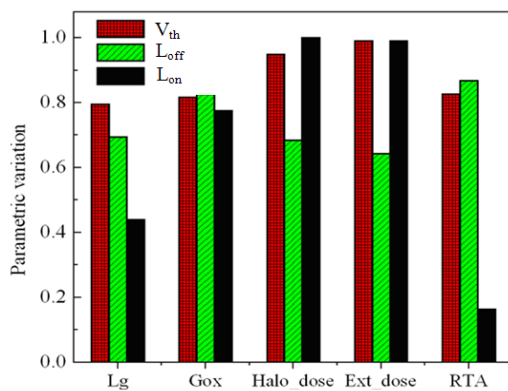


Fig. 9: Sensitivity analysis of process variability for 45 nm process-induced strained-Si MOSFETs

The combination of Sentaurus Process, Sentaurus Device, PCM studio and Sentaurus Workbench, forms a powerful Design for Manufacturing (DFM) TCAD environment. In this study, a total of 1200 experiments were generated. The process and device simulation results are subsequently used as the basis for generating a Process Compact Model (PCM), which encapsulates the relationships between input (design) and output parameters. The PCM automatically correlates design parameters to the tolerances. The ranges are normalized to 1 (Fig. 9), with the center representing the nominal value for each parameter. Table 2 summarizes the parameters and ranges chosen to optimize strain-engineered MOSFETs, including the names used as references in.

The process was optimized with respect to threshold voltage, channel stress, device current and transconductance. Parallel coordinate plots link the simulation results to the design variation. The parameter values and ranges indicate whether the domain has been covered sufficiently. The yellow region is the constraint of the parameters and the outputs that satisfy the range of design specifications. Red lines within this region depict the successful design.

For the case study of p-MOSFET threshold voltage optimization, we allowed a threshold voltage variation within 0.007-0.243 V. We put a variation limit on gate length by narrowing the experiment selection resulting in a 5% lower V_t compared to the nominal value. We select only lower V_t which means reducing on-state voltage. The optimization procedure is continued and finally we perform a further screening on germanium mole fraction for process-induced strain-engineered p-MOSFETs and nitride cap layer for process-induced strain-engineered n-MOSFET, resulting in a combination that gives Ge mole fraction and SiN thickness, generating the optimized V_t . By repeating the above optimization procedure, the device performance may further be improved to obtain V_t within 1%. The process conditions satisfying the specifications for V_t indicated in red in the parallel coordinate plot provides information about how well the domain space is covered with the chosen DoE.

Table 2: Process variability and range considered in PCM studio

Parameters	Parameters name	Variation (%)
Gate length	L_g	± 20
Gate oxide	G_{ox}	± 10
Halo implant dose	Halo_Dose	± 25
Extension implant dose	Ext_Dose	± 15
Peak temperature for RTA	RTA	± 10

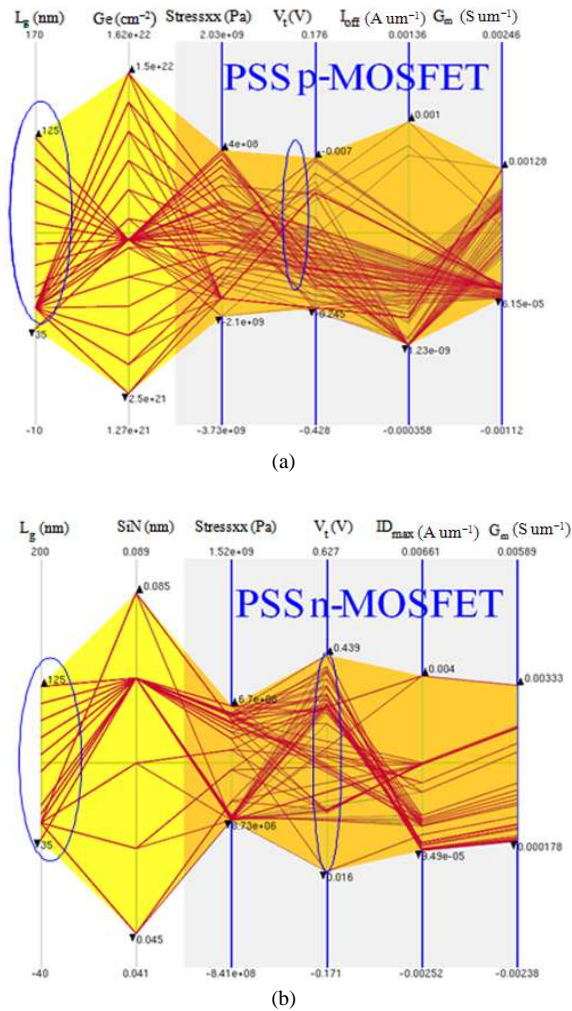


Fig. 10: Parallel coordinate plot. The process is optimized with respect to threshold voltage, current and transconductance for process-induced strained-Si (a) p- and (b) n-MOSFETs

Figure 10a and b show the Process Compact Model (PCM) evaluation scenarios for process-induced strain-engineered p- and n-MOSFETs, respectively. Figure 10a is a parallel coordinate plot that links the simulation results to the design variation of the gate length (L_g) and Germanium mole fraction (Ge) in embedded-SiGe source/drain region for process-induced strain-engineered p-MOSFETs. Similarly, Fig. 10b is a parallel coordinate plot that links the simulation results to the design variation of the gate length (L_g) and cap layer thickness (SiN) for process-induced strain-engineered n-MOSFETs. However, more advanced analyses are possible, including fluctuation analysis of

different fabrication processes, leading towards the optimization of manufacturing yield. The above DFM/PCM simulation example demonstrates how to optimize a process and to reduce the process development time by reducing the number of costly and time consuming design iterations.

CONCLUSION

With extreme scaling down of MOSFETs in high volume manufacturing, it is imperative to develop a systematic TCAD-based methodology to design, characterize and optimize manufacturability to increase yield. Sentaurus Process and Device simulators are used to simulate DC and AC characteristics and Sentaurus Workbench Visualization is used to extract device parameters such as V_{th} , I_{on} , I_{off} and RF parameters. Process Compact Model has been used to find the optimum process conditions to meet a set of device specifications for strain-engineered MOSFETs. The interactive visual optimization process using design of experiments in a parallel coordinate plot allows one to explore device performance criteria. Utilization of TCAD tools for process optimization for overall Design For Manufacturing (DFM) solution is demonstrated.

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REFERENCES

Abdallah, M. and I. Nabhan, 2009. A novel high stop band all complementary MOSFET switched-capacitor filter. Am. J. Eng. Applied Sci., 2: 699-702. <http://www.scipub.org/fulltext/ajeas/ajeas24699-702.pdf>

Fajri, P., S. Afsharnia, D. Nazarpour and M.A. Tavallaei, 2008. Modeling, simulation and group control of distributed static series compensators. Am. J. Eng. Applied Sci., 1: 347-357. <http://www.scipub.org/fulltext/ajeas/ajeas14347-357.pdf>

Ghani, T., M. Armstrong, C. Auth, M. Bost and P. Charvat *et al.*, 2003. A 90nm high volume manufacturing logic technology featuring novel 45nm gate length strained silicon CMOS transistors. Proceeding of the IEEE Technical Digest International Electron Devices Meeting, Dec. 8-10, IEEE Xplore Press, USA., pp: 11.6.1-11.6.3. DOI: 10.1109/IEDM.2003.1269442

Kittel, C., 1987. Quantum Theory of Solid. 2nd Edn., Wiley, Canada, ISBN: 9780471624127, pp: 528.

- Kolomoets, V., V. Baidakov, A. Fedosov, A. Gorin and V. Ermakov *et al.*, 2009. Application of piezoresistance effect in highly uniaxially strained p-Si and n-Si for current-carrier mobility increase. *Phys. Status Solidi*, 246: 3 652-654. DOI: 10.1002/pssb.200880508
- Maiti, C.K., S. Chattopadhyay and L.K. Bera, 2007a. *Strained-Si Heterostructure Field Effect Devices*. 1st Edn., Taylor and Francis, Boca Raton, ISBN: 9780750309936, pp: 423.
- Maiti, T.K., S.S. Mahato, S.K. Sarkar and C.K. Maiti, 2007b. Performance enhancement of p-MOSFETs with embedded SiGe source/drain on hybrid orientation substrates. *Proceedings of the 8th International Conference on Ultimate Integration on Silicon*, Mar. 15-16, Belgium, pp: 1-26.
- Montgomery, D.C., 2000. *Design and Analysis of Experiments*. 5th Edn., Wiley, New York, ISBN: 10: 0471316490, pp: 672.
- Nag, B.R., 2001. *Physics of Quantum Well Devices*. 1st Edn., Springer, USA., ISBN: 10: 0792365763, pp: 308.
- Roblin, P. and H. Rohdin, 2001. *High Speed Heterostructure Devices*. 1st Edn., Cambridge University Press, Cambridge, UK., ISBN: 10: 0521781523, pp: 600.
- Sena, K. and S. Piyasin, 2008. Determination of average contour of Thais skulls for design of implants. *Am. J. Eng. Applied Sci.*, 1: 168-173. <http://www.scipub.org/fulltext/ajeas/ajeas13168-173.pdf>
- Sun, Y., S.E. Thompson and T. Nishida, 2007. Physics of strain effects in semiconductors and metal-oxide-semiconductor field-effect transistors. *J. Applied Phys.*, 101: 1-22. DOI: 10.1063/1.2730561
- Synopsys, 2008a. An advanced 1D, 2D and 3D process simulator. Synopsys. <http://www.synopsys.com/Tools/TCAD/ProcessSimulation/Pages/SentaurusProcess.aspx>
- Synopsys, 2008b. Physics of strain effects in semiconductors and metal-oxide-semiconductor field-effect transistors. Synopsys. <http://www.synopsys.com/Tools/TCAD/DeviceSimulation/Pages/SentaurusDevice.aspx>
- Yeo, Y.C., J. Sun and E.H. Ong, 2004. Strained channel transistor using strain field induced by source and drain stressors. *Mater. Res. Soc. Symp.*, 809: B10.4.1-B10.4.6.